Listing of the Claims:

1. (Previously Presented) An integrated circuit comprising:

a system base chip configured for communicating over a vehicle data bus, the system base chip including, at least

a system voltage supply,

a system reset,

a monitoring function,

an interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol, and in particular the LIN (Local Interconnect Network) protocol, that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte, and

a serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit.

2. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that there is provided in the integrated circuit an R/C oscillator that acts as a clock-signal source and as a timebase for the bit-rate detection.

3. (Previously Presented) An integrated circuit as claimed in claim 2, characterized in that the clock signal generated by the R/C oscillator may also be provided to circuits outside the integrated circuit, and in particular to a microprocessor.

4. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that the interface circuit may also pass on complete messages.

5. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that the interface circuit performs buffer-storage of data received or to be transmitted.

6. (Previously Presented) An integrated circuit as claimed in claim 1, characterized in that the serial/parallel converter converts serial data conforming to the SCI/UART (Serial

Communication Interface/Universal Asynchronous Receiver Transmitter) interface standard into parallel data, or vice versa.

7. (Previously presented) An integrated circuit comprising:

a base chip including one or more circuits configured to

receive a vehicle battery voltage;

convert the vehicle battery voltage to a regulated voltage;

provide the regulated voltage as an output of the integrated circuit;

monitor the vehicle battery voltage;

provide a reset signal in response to the monitoring of the vehicle battery voltage;

receive analog signals from a serial communication interface/universal asynchronous receiver transmitter (SCI/UART) interface, the analog signals corresponding to data formatted for a Local Interconnection Network (LIN) protocol;

identify individual bytes from a digital data signal;

identify a LIN protocol header from at least one of the individual bytes;

detect a bit rate for the received analog signals in response to the detected LIN protocol header and with reference to a clock signal;

convert the analog signals to a digital data signal in response to the detected bit rate;

perform a serial to parallel conversion on the digital data signal; and

provide the parallel-converted digital data signal as an output of the integrated circuit.

8. (Previously Presented) The integrated circuit of claim 7, wherein the one or more circuits are further configured to

receive data from a parallel bus input to the integrated circuit;

convert the data from the parallel bus input to a serial form; and

transmit the serial form of the data from the parallel bus input on the SCI/UART interface in response to the detected bit rate.

9. (Previously Presented) The integrated circuit of claim 7, wherein the one or more circuits are further configured to provide a watchdog function and in response to the watchdog function provide an interrupt as an output of the integrated circuit.

10. (Previously Presented) The integrated circuit of claim 7, wherein the base chip further includes a resistor-capacitor (RC) clock generation circuit that is configured to provide the clock signal.